IN THE CLAIMS

1-4. (Canceled)

5. (Currently Amended) A memory system comprising:

a memory controller;

a separate unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a separate bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation; and

a plurality N of pipelined memory subsystems, wherein each memory subsystem includes:

a plurality M of memory devices wherein each memory device internally contains a data in and a data out buffer directly connected to the separate bidirectional data bus, a column decoder and a row decoder;

a command buffer directly connected between the separate unidirectional command and address bus and the plurality of memory devices, the command buffer receiving and latching the commands and addresses from the separate unidirectional command and address bus and driving the commands and addresses to the plurality of memory devices, wherein the command buffer is shared by the plurality of M memory devices in the memory subsystem; and

a data buffer directly connected between the plurality of M memory devices and the separate bidirectional data bus, the data buffer receiving and latching the data information from the separate bidirectional data bus and driving the data information to the plurality of M memory devices for a write operation, the data buffer receiving and latching the data information from the plurality of M memory devices and driving the data information to the separate bidirectional data bus for a read operation, wherein the data buffer is shared by the plurality of M memory devices in the memory subsystem.

6. (Previously Presented) The memory system according to claim 5, wherein the memory controller communicates the commands and addresses and the data information using a pipelined packet-protocol which incorporates a first delay introduced by the command buffer of one of the plurality of pipelined memory subsystems and a second delay introduced by the data buffer of one of the plurality of pipelined memory subsystems.

7. (Original) The memory system according to claim 5 wherein each memory device is a dynamic random access memory device.

8. (Original) The memory system according to claim 5 wherein each of the plurality N of pipelined memory subsystems includes eight memory devices and wherein N equals eight.

9-28. (Canceled)

29. (Currently Amended) A method of retrieving data in a pipelined memory system, having a plurality of memory subsystems, wherein each memory subsystem includes a command buffer, a data buffer and a plurality of memory devices, wherein each memory device includes addressable storage, a data in and a data out buffer, a column decoder and a row decoder, comprising:

issuing commands and addresses on a separate unidirectional command and address bus;

latching the commands and addresses in the command buffers of each memory subsystem, wherein each of the command buffers is shared by M of the plurality of memory device of each memory subsystem and is positioned between and is directly connected to, ~~the command~~ the command and address bus and the plurality of M memory devices of each memory subsystem;

driving the latched commands and addresses to the column and row decoders;

retrieving data from the addressable storage of one of the plurality of memory devices;

latching the data in the data in and data out buffer of the one of the plurality of memory devices;

latching the data in the data buffer of the one memory subsystem; and

receiving the data on a bidirectional data bus.

30. (Previously Presented) The method of retrieving data according to claim 29 wherein each of the memory devices is a dynamic random access memory device.

31. (Previously Presented) The method of retrieving data in a pipelined memory system according to claim 29 wherein issuing commands and addresses and receiving data communicates according to a packet protocol which incorporates a first delay introduced by the command buffer and a second delay introduced by the data buffer.

32. (Currently Amended) A method of storing data in a pipelined memory system, having a plurality of memory subsystems, wherein each memory subsystem includes a command buffer, a data buffer and a plurality of memory devices, wherein each memory device includes addressable storage, a data in and a data out buffer, a column decoder and a row decoder, comprising:

issuing commands and addresses on a separate unidirectional command and address bus;

issuing data on a bidirectional data bus;

latching the commands and addresses in the plurality of command buffers, wherein each of the plurality of command buffers is shared by M of the plurality of memory devices and is positioned between, and directly connected to, the separate unidirectional command and address bus and the plurality of memory devices;

latching the data in the plurality of data buffers of the memory subsystem;

driving the latched commands and addresses to the column and row decoders;

driving the latched data to the data in buffers of the memory device; and

storing the data in the addressable storage of the plurality of memory devices.

33. (Previously Presented) The method of claim 32, wherein issuing commands and addresses and issuing data include executing a packet protocol which incorporates a first delay

introduced by the command buffer of one of the plurality of memory subsystems and a second delay introduced by the data buffer of one of the plurality of memory subsystems.

34. (Currently Amended) An electronic system comprising:

a microprocessor;

a memory controller coupled to the microprocessor;

a separate unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the unidirectional command and address bus;

a separate bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the separate bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation; and

a plurality N of pipelined memory subsystems, wherein each memory subsystem includes:

a plurality M of memory devices wherein each memory device internally contains a data in and a data out buffer, a column decoder and a row decoder;

a command buffer, directly connected to the separate unidirectional command and address bus, and connected between the command and address bus and the plurality of memory devices, the command buffer receiving and latching the commands and addresses from the separate command and address bus and driving the commands and addresses to the plurality of memory devices, wherein the command buffer is shared by the plurality of memory devices; and

a data buffer connected between the plurality of memory devices and the separate bidirectional data bus, and directly connected to the separate bidirectional data bus, the data buffer receiving and latching the data information from the separate bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data buffer receiving and latching the data information from the plurality of memory devices and driving the data information to the separate bidirectional data bus for a read operation.

35. (Previously Presented) The electronic system of claim 34, wherein the memory controller communicates the commands and addresses and data information using a pipelined packet-protocol which incorporates a first delay introduced by the command buffer of one of the plurality of pipelined memory subsystems and a second delay introduced by the data buffer of one of the plurality of pipelined memory subsystems.

36. (Previously Presented) The electronic system of claim 34, wherein each memory device is a dynamic random access memory device.

37. (Previously Presented) The electronic system of claim 34, wherein both M and N equal eight.

38. (Currently Amended) A method of performing a memory transaction in an electronic system having a memory controller and a plurality of memory subsystems, wherein each memory subsystem includes a command buffer, a data buffer and a plurality of memory devices, wherein each memory device internally includes a data in and a data out buffer, a column decoder and a row decoder, comprising:

issuing information to the memory controller;

issuing commands and addresses on a separate unidirectional command and address bus;

issuing data on a separate bidirectional data bus;

latching the commands and addresses received from the separate unidirectional command and address bus in the command buffers of the plurality of memory subsystems, wherein each of the command buffers is shared by the plurality of memory device of each memory subsystem and is positioned directly between ~~the command~~ the command and address bus and the plurality of memory devices of each memory subsystem;

driving the latched commands and addresses to the plurality of memory devices; and

if the memory transaction is a write, receiving and latching the data in the data buffers of the plurality of memory subsystems, driving the latched data to the data in and data out buffer, and writing the data to an addressed memory storage of the plurality of memory devices.

39. (Previously Presented) The method of claim 38, wherein issuing commands and addresses and issuing data include executing a packet protocol which incorporates a first delay introduced by the command buffer and a second delay introduced by the data buffer.

40. (Currently Amended) A method of storing data, in an electronic system, having a memory controller and a plurality of memory subsystems, wherein each memory subsystem includes a command buffer, a data buffer and a plurality of memory devices, wherein each memory device internally includes a data in and a data out buffer, a column decoder and a row decoder, comprising:

issuing information to the memory controller, wherein the memory controller receives the information and wherein the memory controller issues commands and addresses on a separate unidirectional command and address bus;

issuing data on a separate bidirectional data bus;

latching the commands and addresses read from the separate unidirectional command and address bus in the command buffers of the plurality of memory subsystems, wherein each of the command buffers is shared by the plurality of memory device of each memory subsystem and is positioned directly between the separate unidirectional command ~~the command~~ and address bus and the plurality of memory devices of each memory subsystem;

latching the data received from the separate bidirectional data bus in the data buffers of the plurality of memory subsystems;

driving the latched commands and addresses to the plurality of memory devices;

driving the latched data to the data in and data out buffer of the plurality of memory devices; and

storing the data from the data in and data out buffer in addressable storage of the plurality of memory devices.

41. (Previously Presented) The method of claim 40, wherein issuing commands and addresses and issuing data include executing a packet protocol which incorporates a first delay introduced by the command buffer and a second delay introduced by the data buffer.

42. (Currently Amended) In an electronic system having a memory controller and a plurality of memory subsystems, wherein each memory subsystem includes a command buffer, a data buffer and a plurality of memory devices, wherein each memory device internally includes a data in and a data out buffer, a column decoder and a row decoder, a method of retrieving data comprising:

issuing information to the memory controller;

issuing commands and addresses on a separate unidirectional command and address bus;

latching the commands and addresses read from the separate unidirectional command and address bus in the command buffers of the plurality of memory subsystems, wherein each of the command buffers is shared by the plurality of memory device of each memory subsystem and is positioned directly between the separate unidirectional command the command and address bus and the plurality of memory devices of each memory subsystem;

driving the latched commands and addresses to the plurality of memory devices of the plurality of memory subsystems;

retrieving data from addressable storage of the plurality of memory devices of the plurality of memory subsystems;

latching the data in the data in and data out buffer of a memory storage device;

latching the data in the data buffers of the plurality of memory devices of the plurality of memory subsystems; and

receiving the data on a separate bidirectional data bus.

43. (Previously Presented) The method of claim 42, wherein issuing commands and addresses and receiving data include executing a packet protocol which incorporates a first delay introduced by the command buffer and a second delay introduced by the data buffer.

44. (Currently Amended) A memory system comprising:

a separate unidirectional command and address bus coupleable to a memory control device;

a separate bidirectional data bus coupleable to the memory control device; and

a plurality N of pipelined memory subsystems, wherein each memory subsystem includes:

a plurality M of memory devices, wherein each memory device internally contains a data in and a data out buffer, a column decoder and a row decoder;

a command buffer directly connected between the separate unidirectional command and address bus and the plurality of memory devices, the command buffer receiving and latching commands and addresses from the separate unidirectional command and address bus and driving the commands and addresses to the plurality of memory devices, wherein the command buffer is shared by the plurality of memory devices; and

a data buffer connected between the plurality of memory devices and the separate bidirectional data bus, the data buffer receiving and latching data information from the separate bidirectional data bus and driving the data information to data in and data out buffer of the plurality of memory devices for a write operation, the data buffer receiving and latching the data information from the data in and data out buffer of the plurality of memory devices and driving the data information to the separate bidirectional data bus for a read operation.

45. (Previously Presented) The memory system of claim 44, wherein the commands and addresses and the data information communicate using a pipelined packet-protocol which incorporates a first delay introduced by the command buffer register of one of the plurality of pipelined memory subsystems and a second delay introduced by the data buffer of one of the plurality of pipelined memory subsystems.

46. (Previously Presented) The memory system of claim 44, wherein each memory device is a dynamic random access memory device.

47. (Previously Presented) The memory system of claim 44, wherein both M and N equal eight.

48. (Currently Amended) A method of storing data in a pipeline memory system, having a plurality of memory subsystems, wherein each memory subsystem includes a command buffer, a data buffer and a plurality of memory devices, wherein each memory device internally includes addressable storage, a data in and a data out buffer, a column decoder and a row decoder, comprising:

receiving commands and addresses from a separate unidirectional command and address bus;

receiving data from a separate bidirectional data bus;

latching the commands and addresses in the plurality of command buffers, wherein each command buffer is directly connected to the separate unidirectional command and address bus;

latching the data in the plurality of data buffers;

driving the latched commands and addresses to the column and row decoders;

driving the latched data to the data in buffers; and

storing the data latched in the data in buffer in the addressable storage of the plurality of memory devices.

49. (Previously Presented) The method of claim 48, wherein receiving commands and addresses and receiving data include executing a packet protocol which incorporates a first delay introduced by the command buffer and a second delay introduced by the data buffer.

50. (Currently Amended) A method of retrieving data in a pipeline memory system, having a plurality of memory subsystems, wherein each memory subsystem includes a command buffer, a data buffer and a plurality of memory devices, wherein each memory device internally includes addressable storage, a data in and a data out buffer, a column decoder and a row decoder, comprising:

receiving commands and addresses from a separate unidirectional command and address bus;

latching the commands and addresses in the plurality of command buffers directly connected to the separate unidirectional command and address bus;

driving the latched commands and addresses to the column and row decoders;

retrieving data from the addressable storage of the plurality of memory devices;

latching the data in the data in and data out buffer of the memory device;

latching the data from the data in and data out buffer in the plurality of data buffers; and

driving the data from the data in and data out buffer onto a data bus.

51. (Previously Presented) The method of claim 50, wherein receiving commands and addresses and driving the data include executing a packet protocol which incorporates a first delay introduced by the command buffer and a second delay introduced by the data buffer.

52. (Currently Amended) A memory system, comprising:

a separate unidirectional command and address bus in electrical communication with a memory control device;

a separate bidirectional data bus in electrical communication with the memory control device; and

a plurality N of pipelined memory subsystems, wherein each memory subsystem includes:

a plurality M of memory devices, wherein each memory device internally contains a data in and a data out buffer, a column decoder and a row decoder;

a command buffer directly connected to the separate unidirectional command and address bus, and connected between the separate unidirectional command and address bus and the plurality of memory devices, the command buffer receiving and latching commands and addresses from the separate unidirectional command and address bus and driving the commands and addresses to the plurality of memory devices, wherein the command buffer is shared by the plurality of memory devices; and

a data buffer connected between the data in and data out buffer of each of the plurality of memory devices and the separate bidirectional data bus, the data buffer receiving and latching data information from the separate bidirectional data bus and driving the data information to the data in and data out buffer of the plurality of memory devices for a write operation, the data buffer receiving and latching the data information from the data in and data out buffer of the plurality of memory devices and driving the data information to the separate bidirectional data bus for a read operation, wherein the data buffer is directly connected to the separate bidirectional data bus.

53. (Previously Presented) The memory system of claim 52, wherein the commands and addresses and the data information communicate using a pipelined packet-protocol which incorporates a first delay introduced by the command buffer of one of the plurality of pipelined memory subsystems and a second delay introduced by the data buffer of one of the plurality of pipelined memory subsystems.

54. (Previously Presented) The memory system of claim 52, wherein each memory device is a dynamic memory device.

55. (Previously Presented) The memory system of claim 52, wherein both N and M equal eight.

56. (Currently Amended) A method of retrieving data in a pipelined memory system, comprising:

issuing commands and addresses on a separate unidirectional command and address bus to a plurality of memory subsystems;

latching the commands and addresses in a command buffer in each of the plurality of memory subsystems;

driving the latched commands and addresses to column and row decoders in each of the plurality of subsystems;

retrieving data from addressable storage of only one of the plurality of memory subsystems;

latching the data in a data buffer of the one of the plurality of memory subsystems; and

receiving the data on a separate bidirectional data bus.

57. (Currently Amended) A memory system comprising:

a memory controller;

a separate unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the separate unidirectional command and address bus;

a separate bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the separate bidirectional data bus for a write operation and receiving the data information from the separate bidirectional data bus during a read operation; and

a plurality N of pipelined memory subsystems, wherein each memory subsystem includes:

a plurality M of memory devices wherein each memory device internally consists of a data in and a data out buffer, a decoder and an array of memory cells;

a command buffer directly connected between the separate unidirectional command and address bus and the plurality of memory devices, the command buffer receiving and latching the commands and addresses from the separate unidirectional command and address

bus and driving the commands and addresses to the plurality of memory devices, wherein the command buffer is shared by the plurality of memory devices; and

a data buffer directly connected between the plurality of memory devices and the separate bidirectional data bus, the data buffer receiving and latching the data information from the separate bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data buffer receiving and latching the data information from the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation.

58. (Previously Presented) The memory system of claim 57, wherein the data buffer is shared by the plurality of memory devices.

59. (Previously Presented) The memory system of claim 5, wherein N equals eight.

60. (Previously Presented) The memory system of claim 5, wherein M equals eight.

61. (Previously Presented) The memory system of claim 5, wherein each of the memory devices includes an addressable storage.

62. (Previously Presented) The system according to claim 5, wherein the bidirectional data bus is a single 16 bit bus, supports 64 data buffers, and operates at 800 MHz.

63. (Previously Presented) A method of operating the memory system of claim 5, comprising:

issuing commands and addresses on the unidirectional command and address bus;

latching the commands and addresses in the command buffers;

driving the latched commands and addresses to the column and row decoders;

retrieving data from addressable storage of one of the plurality of memory devices;

latching the data in the data in and data out buffers;

latching the data from the data in and data out buffer in the data buffers; and

receiving the data on the bidirectional data bus.

64. (Previously Presented) The electronic system of claim 34, wherein the data buffer is shared by the plurality of memory devices.

65. (Previously Presented) The memory system of claim 44, wherein the data buffer is shared by the plurality of memory devices.

66. (Previously Presented) The memory system of claim 52, wherein the data buffer is shared by the plurality of memory devices.

67. (Currently Amended) A memory system comprising:

a memory controller;

a separate unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the separate unidirectional command and address bus;

a separate bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the separate bidirectional data bus for a write operation and receiving the data information from the separate bidirectional data bus during a read operation; and

a plurality N of pipelined memory subsystems, wherein each memory subsystem includes:

a plurality M of memory devices, wherein each memory device internally contains a data in and a data out buffer, a column decoder and a row decoder;

a command buffer directly connected between the separate unidirectional command and address bus and the plurality of memory devices, the command buffer receiving and latching the commands and addresses from the separate unidirectional command and address bus and driving the commands and addresses to the plurality of memory devices; and

a data buffer directly connected between the plurality of memory devices and the separate bidirectional data bus, the data buffer receiving and latching the data information from the separate bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data buffer receiving and latching the data information from the plurality of memory devices and driving the data information to the separate bidirectional data bus for a read operation, wherein the data buffer is shared by the plurality of memory devices.

68. (Previously Presented) The memory system according to claim 67, wherein the memory controller communicates the commands and addresses and the data information using a pipelined packet-protocol which incorporates a first delay introduced by the command buffer of one of the plurality of pipelined memory subsystems and a second delay introduced by the data buffer of one of the plurality of pipelined memory subsystems.

69. (Previously Presented) The memory system according to claim 67, wherein each memory device is a dynamic random access memory device.

70. (Previously Presented) The memory system according to claim 67, wherein each of the plurality N of pipelined memory subsystems includes eight memory devices and wherein N equals eight.

71. (Previously Presented) The system according to claim 67, wherein the bidirectional data bus is a single 16 bit bus, supports 64 data buffers, and operates at 800 MHz.